though benzene is preferentially adsorbed. If counterdiffusion could occur, mesitylene should be able to displace essentially all the presorbed 1,3,5-triisopropyl benzene in NaY. On the other hand, when equilibrium permits counterdiffusion to occur in the zeolite pores, presorbed molecules with relatively small critical diameters are readily desorbed regardless of the size of the incoming molecules, provided the latter are capable of entering the pore mouths. Examples are the counterdiffusion of cyclohexane from NaY into mesitylene or into 1,3,5-triisopropyl benzene.

It appears that when molecules with critical diameters that are large relative to the zeolite pores are occluded, their mobilities in the zeolite channels are greatly reduced due to geometrical obstructions and strong interactions between the molecule and the zeolite wall. The interactions between incoming and outgoing molecules can further immobilize the presorbed molecules to the point that counterdiffusion becomes imperceptively slow.

ACKNOWLEDGMENT

This work was supported by the National Science Foundation under Grant GK-1707. The zeolite was supplied by the Linde Division of the Union Carbide Corporation.

NOTATION

D_E = effective diffusion coefficient, cm^2/s
M_t = amount of mass diffused in at time t
M_∞ = amount of mass diffused in after infinite time
t = time, s

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HI-H_2 Vapor Etch for Low Temperature Silicon Epitaxial Manufacturing

Etching of semiconductor silicon slices at 998°C with HI-H_2 mixtures was developed to the level that practical etch rates ($\geq$ 0.1 μm/min) and smoothness of surfaces were obtained in a manufacturing type reactor without the addition of HF or He. Such a low temperature etch is expected to lead to improved device characteristics, mainly because of more sharply defined junction surfaces.

Using deposition at 998°C on very clean slices as a testing method, two sources of impurities that cause stacking faults in the deposition layers were identified and eliminated. These were the polypropylene vessel used in the slice cleanup procedure, and the hydrogen peroxide used in conjunction with sulfuric acid in the primary cleaning step.

LAWRENCE D. DYER

Chemical Materials Division
Texas Instruments, Inc.
Dallas, Texas 75222

SCOPE

Modern electronic systems increasingly demand improvements in the performance, reliability, and cost of solid state devices. Many current limitations of systems relate directly to device limitations; of particular concern is speed of operation. The ability to produce improved devices has reached a state of the art where possibly the most significant advances will be made in the area of materials processing.

Lowering the temperature of solid state device processing would have particularly beneficial effects: more sharply defined junction interfaces would be possible, allowing higher device speeds; more freedom from crystal

defects would result, giving higher yields and reliabilities.

The objective of this study was to establish one of the techniques necessary for achieving low temperature (< 1,000°C) deposition of device quality silicon on silicon substrates—low temperature vapor etching. The study necessarily concerns the slice cleanup procedure and the silicon deposition process and optical microscopy of the surfaces produced.

Previous work by Richman (1969), Dismukes (1970), and Levin et al. (1971) showed that HI-HF-H_2 mixtures were capable of smooth etching of silicon down to 900°C in a two-slice reactor of special design; however, it was necessary to add helium to achieve reproducible, practical etch rates.

CONCLUSIONS AND SIGNIFICANCE

Etching of semiconductor silicon slices at 998°C with HI/H_2 mixtures was developed to the level that practical etch rates and smoothness of surfaces were obtained in a manufacturing type reactor without the addition of HF or He.

The etch rate and appearance of silicon surfaces etched at 998°C with HI were found to vary according to the severity of contamination, and this variance yielded a cor-

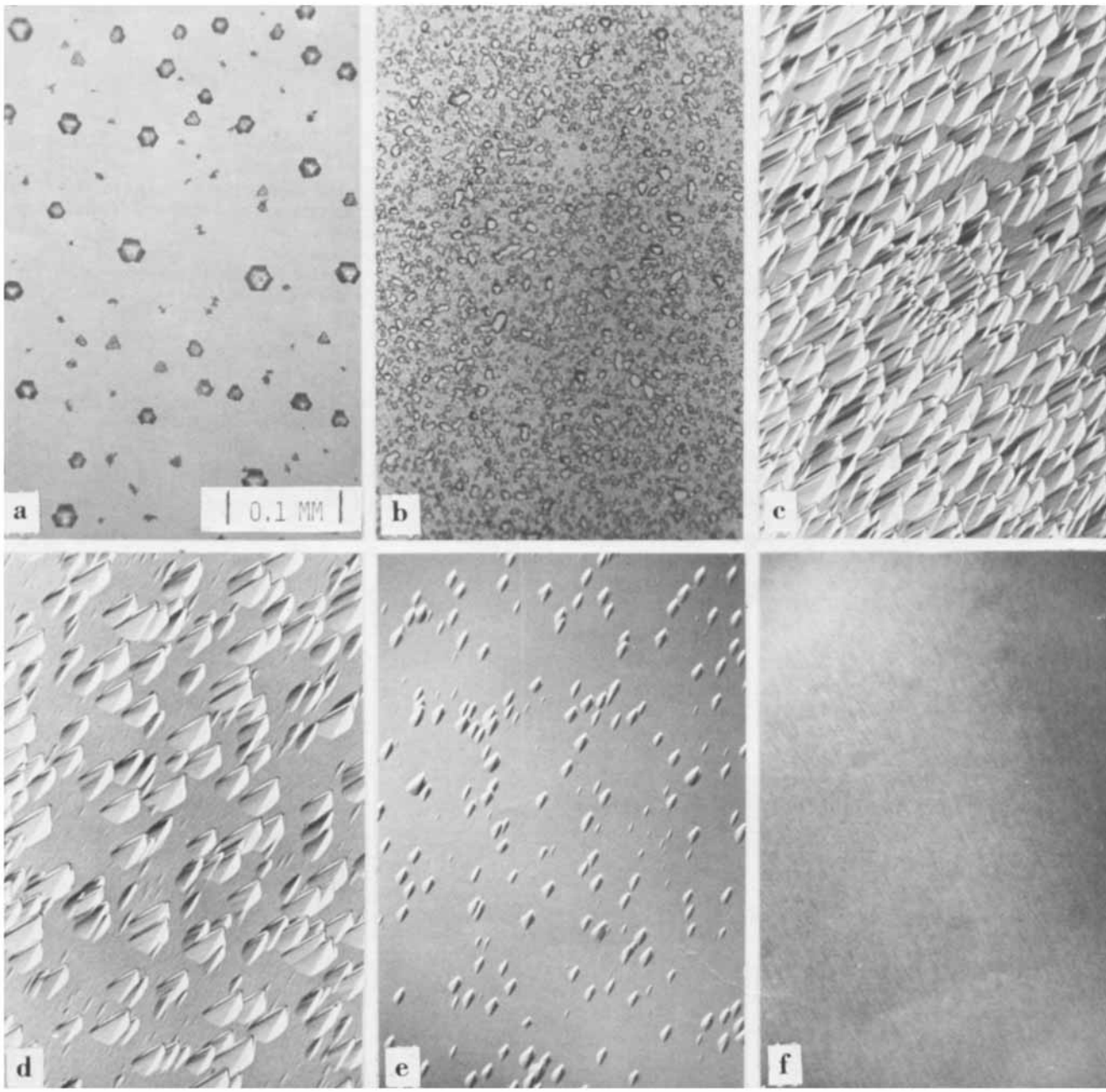


Fig. 1. Increasing uniformity of removal of 1 to 2 μm of silicon by 1.0% HI at 998°C with decreasing amount of surface impurities (interference contrast).

responding variation in stacking fault count in layers deposited at 998°C.

One source of the scatter in etch rates was found to be the variation in time of exposure to rinse water in the cleanup procedure. By minimizing or deleting the water rinse after dilute HF treatment, the etch rate R of {111} silicon with HI/H_2 mixtures could be confined within the bounds $0.1 \leq R \leq 0.23$ μm/min · % HI.

It was shown that commercially available HI could be used for vapor etching of silicon at 998°C without contributing to the stacking fault count in epitaxial layers deposited at 998°C after vapor etching. However, with the cleaning process as it is presently constituted, 998°C HI etching still leaves stacking fault-causing impurities from the cleanup procedure, resulting in a stacking fault count of 1,000 to 5,000/cm². The deposition process itself at 998°C and in a manufacturing type reactor was shown to be satisfactory with regard to crystal perfection.

Two sources of contamination were found in the cleanup procedure that cause stacking faults in the 998°C deposited layers. These were the polypropylene vessel in which the slices were rinsed and the hydrogen peroxide used in conjunction with sulfuric acid in the primary cleaning step. The contamination from these sources did not result in stacking faults, however, if the slices were vapor etched at 1200°C with HCl prior to deposition.

The principal significance of these findings is that a low temperature epitaxial manufacturing process can be considered to be operational as soon as a slice cleanup procedure is found that will reduce the stacking-fault count from the 1,000 to 5,000/cm² level down to the 100-200/cm² level in deposited layers.

APPARATUS, MATERIALS, AND PROCEDURE

Silicon slices were obtained from <111> Czochralski-grown crystals. These were polished on one side in the conventional manner. Electronic grade liquid reagents were used throughout the slice cleanup procedure, which consisted unless otherwise specified of immersing the slice: 1. 5 min in 10 parts H_2SO_4—4 parts 30% H_2O_2; 2. 15 min in running DI water; 3. 1 min in a 5% HF solution; and 4. 15 min in running DI water. Any gaseous etching or epitaxial deposition of silicon was carried out in a commercial vertical-type reactor, obtained from Applied Materials Technology, Inc. Typical deposition rates were 0.3 μm/min using silane. The slices were heated on a graphite susceptor that had been coated with silicon carbide and silicon.

The silane used in deposition was a commercially available 500 ohm-cm grade. The hydrogen gas used was passed through a platinum catalyst bed to convert any oxygen to water, and through a molecular sieve trap to remove the water. A moisture monitor on the hydrogen line showed that the water content was always ≤ 2 ppm. The hydrogen contained about 1,000 ppm N_2 as shown by gas chromatography. The HI and HF purities were 99.7% and 99.9% respectively. The liquid HI had a typical analysis of 99.7% HI, 0.145% H_2, $< 0.005\%$ air, $< 0.002\%$ CO_2, $< 0.060\%$ CH_3I, $< 0.13\%$ benzene, $< 0.004\%$ xylene, $< 0.0015\%$ C_2H_5I, $< 0.0008\%$ C_3H_7I and $< 0.00006\%$ C_4H_9I. Of course, the concentrations of impurities in the gas phase would be much lower.

The experiments were carried out in three stages. First, a set of vapor etching experiments was carried out with the purpose of observing the character and progression of etching and for measuring by weight loss the etch rates in HI/H_2 and $HI/HF/H_2$ mixtures. Some work was also done in improving the reproducibility of these rates. Second, very clean slices were obtained by vapor etching with HCl, at 1,200°C, such that epitaxial deposition at 998°C gave no stacking faults or tripyramids. A test of the HI itself as a cause of contamination was carried out by etching with HI and depositing at 998°C, after the cleaning treatment at 1,200°C. Third, using the very clean slices, various steps in the cleaning procedure were tested. Slices were either immersed in the reagent or dipped part way for a known time, then vapor etched with HI at 998°C and a 4 μm layer was deposited from a silane-hydrogen mixture. Stacking fault and tripyramid distributions and counts were then recorded.

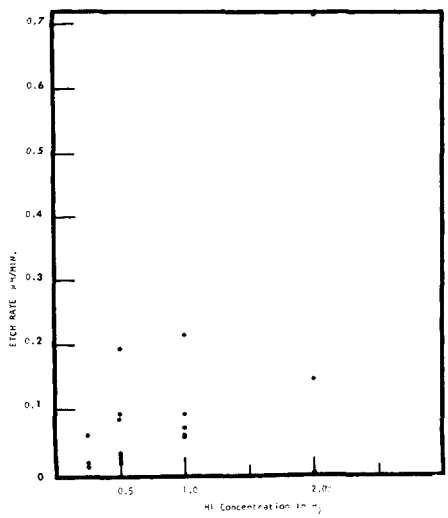


Fig. 2. Etch rate of {111} silicon slices at 998°C versus HI concentration in H_2.

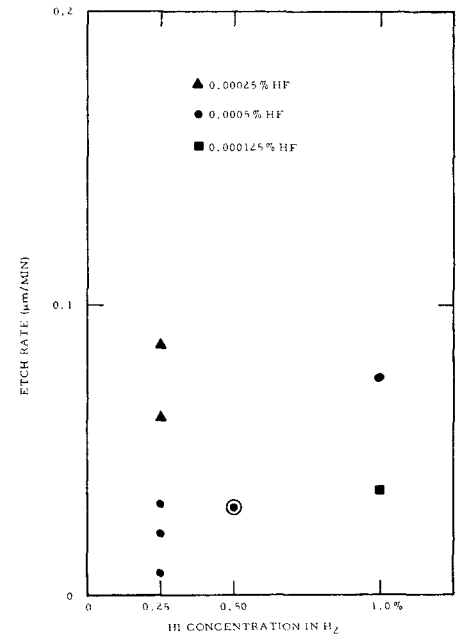


Fig. 3. Etch rate of {111} silicon slices at 998°C versus HI/HF concentration in H_2.

RESULTS

General Progression of Vapor Etching with HI

The progression of etching at 998°C from slight to acceptable is shown in Figure 1. The sequence of micrographs shows increasing uniformity of removal of 1 to 2 μm depending on the extent of absence of surface impurities. If the surface is highly contaminated, the HI/H_2 etch makes only triangular or hexagonal holes (Figure 1a) in the silicon. With more severe attack, such holes become close enough to join together (Figure 1b). More complete etching (Figure 1c) reveals features similar to geological outcroppings, which with improved cleanliness become fewer (Figures 1d, and 1e) and finally disappear (Figure 1f).

Etch Rate Measurements

The rate measurements are given in Figures 2 and 3 for HI/H_2 and $HI/HF/H_2$, respectively. Four different HI concentrations—0.25, 0.50, 1.0, and 2.0%— and three HF concentrations—0.000125, 0.00025, and 0.0005%—were used.

In general the etch rates were quite variable, although the HI/H_2 results were more consistent. From these preliminary studies it could be concluded that the HI/H_2 mixture at 998°C removes most of the surface film and that HF may not be needed.

The appearance of the etched surfaces varied considerably as indicated in Figure 4 which shows surfaces etched at 998°C with 0.5% HI. However, it was noted that 1% mixtures generally gave surfaces freer from outcrops than did 0.25, 0.50, or 2.0% mixtures. Consequently, most of the remaining work was performed with the 1% HI etch.

It was discovered that the rate of etching of silicon by 1% HI in H_2 fell off with increasing water rinse time in the final slice-cleaning step. Figure 5 shows etch rate versus time of exposure to neutral acidity water. The lower times were obtained either by removing the slice directly from the dilute HF or by plunging a slice into DI water. The rate fell by a factor of 2 to 4 in increasing from 0.01 min to 100 min washing time. Thus, it is possible to remove some of the variability in vapor etch rate by controlling the water rinse time, or preferably by deleting the water rinse entirely.

To obtain surfaces which were not subject to contamination arising from the standard cleaning steps, a series of etch-rate measurements was made on slices that had been precleaned at 1,200°C with HCl gas, weighed in air, and returned to the reactor for etching at 998°C with HI. In

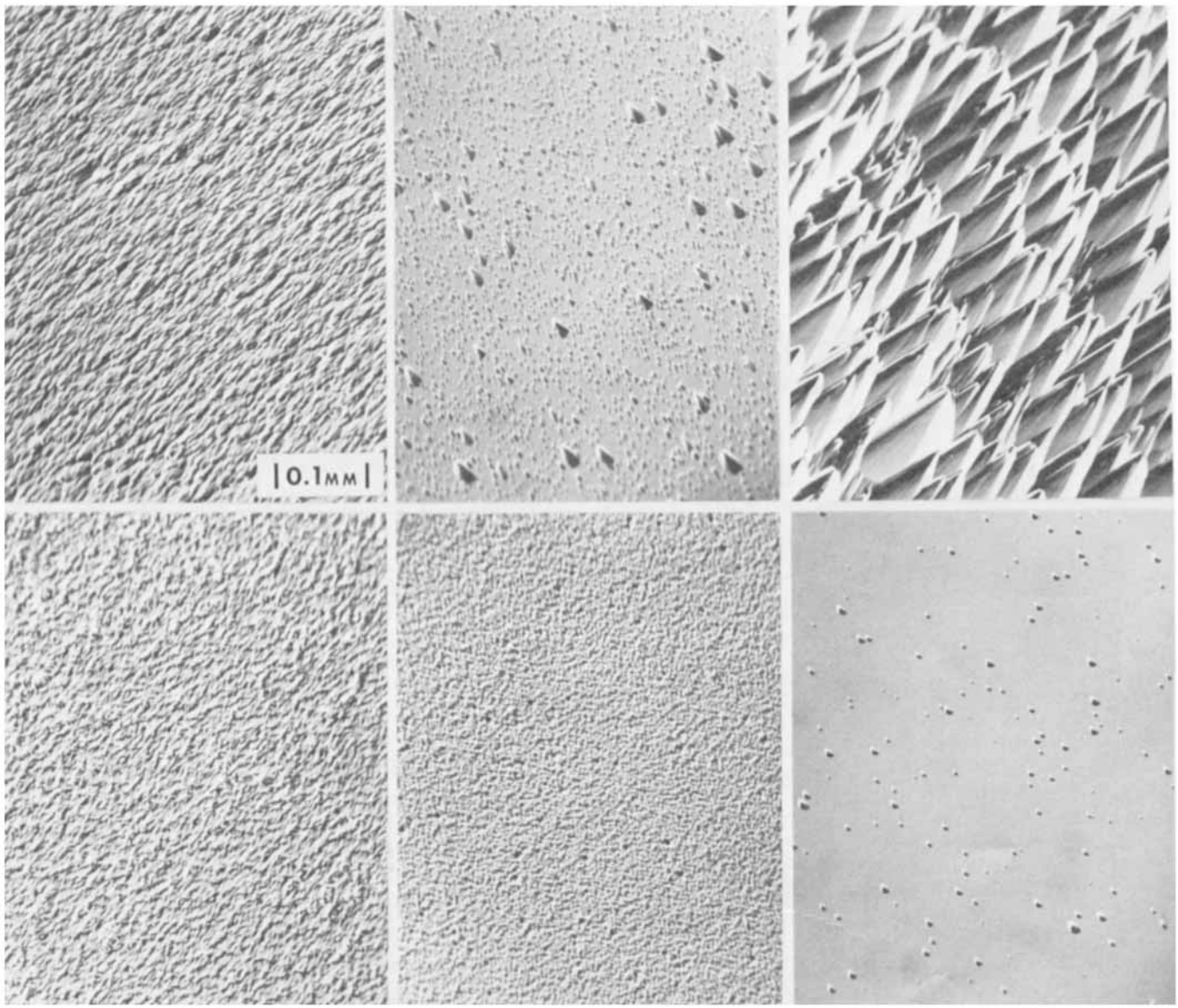


Fig. 4. Variability in appearance of {111} silicon slices etched at 998°C in 0.5% HI in H_2 (interference contrast).

this case the amount of contamination was greatly reduced, as shown by the fact that stacking fault-free silicon could be deposited at 998°C after such treatment. Considerable scatter in the etch rate data still existed, as shown in Figure 6. However, the rates R all fell between two lines: $R = 1.0$ [HI] and $R = 2.33$ [HI], where R is in μm/min and [HI] is the percent HI in H_2. Also, the microscopic appearance of the surfaces after etching was much more consistent with the 1,200°C HCl precleaning than without, as shown in the four runs represented in Figure 7.

Defects Remaining

It was noticed that what seemed to be small bits of particulate impurity were often associated with the tips of outcroppings, and that sometimes parts of the original surface were located there also. Figures 4 and 9 show respectively such parts of the surface. Since the addition of HF was not effective in removing such bits and patches, and since the attack on the patches was from the side rather than from the top, it was concluded that some other impurity present on the surface, besides the oxide formed at room temperature, was responsible for all the outcroppings.

The outcroppings remaining after etching are particularly significant to device manufacture at low temperatures, because any stacking faults or tripyramids in layers

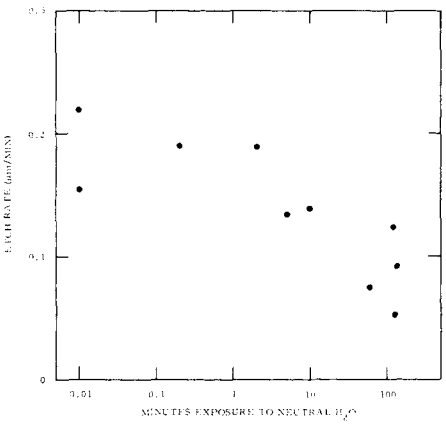


Fig. 5. Etch rate of silicon by 1% HI in H_2 at 998°C versus time of exposure to neutral acidity water.

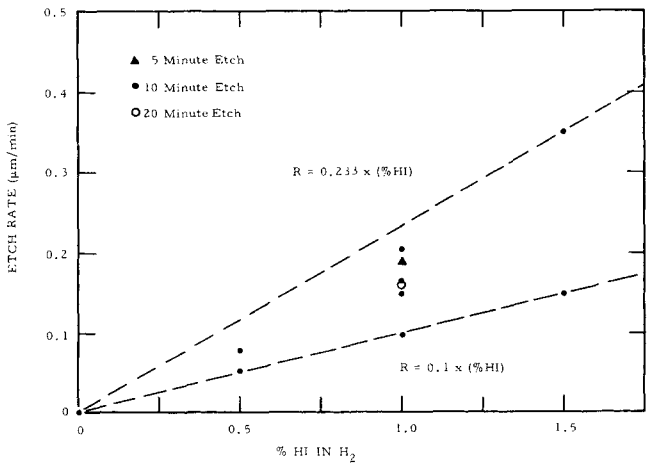


Fig. 6. Etch rate at 998°C of {111} silicon slices precleaned at 1,200°C with HCl versus HI concentration in H_2.

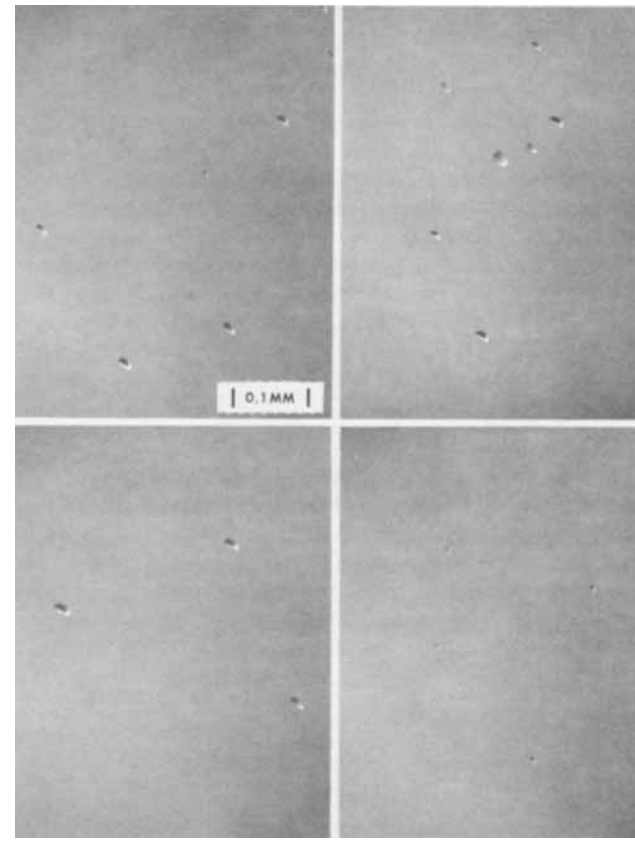


Fig. 7. Appearance of {111} silicon slices etched at 998°C in 1.0% HI in H_2 after 1,200°C HCl pretreatment.

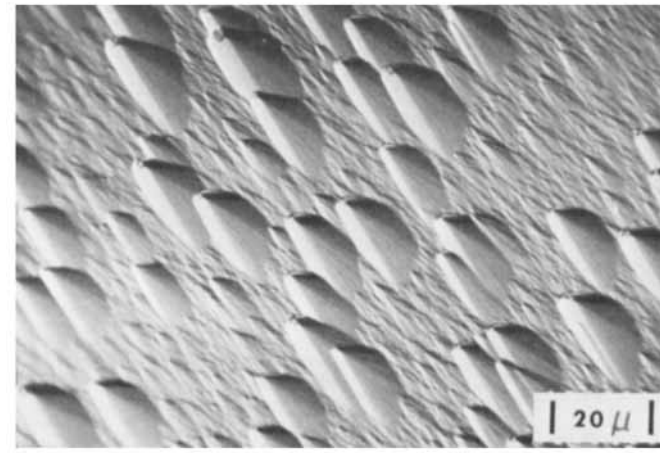


Fig. 8. Bits of particulate matter or unattacked surface at the tips of outcroppings remaining atfer etching at 998°C with HI/H_2 (interference contrast).

deposited at 998°C are found to originate at one of these out-croppings. Figure 10 shows two views of the same area, one in bright field and the other in interference contrast, of a slice etched with HI and deposited at 998°C. The epitaxial layer has been etched 1 min in a CrO_3-HF mixture (Sirtl and Adler, 1961) to reveal stacking faults. It can be seen that not all the outcroppings caused stacking faults, but that any faults that exist are associated with one of the outcroppings.

Deposition Test of Slices Cleaned at 1200°C With HCl

Slices that were cleaned by etching at 1,200°C with HCl showed no stacking faults or tripyramids in epitaxial

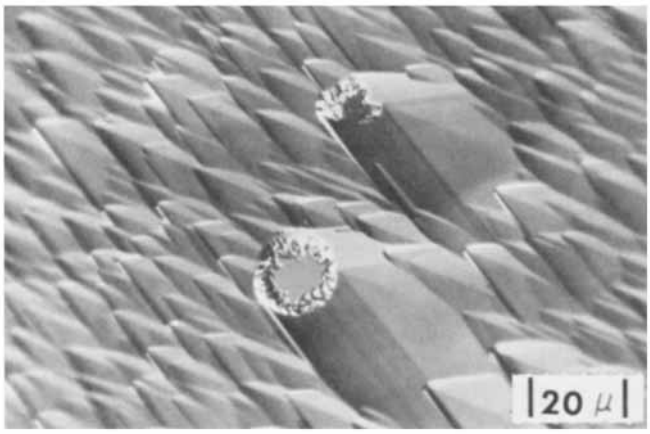
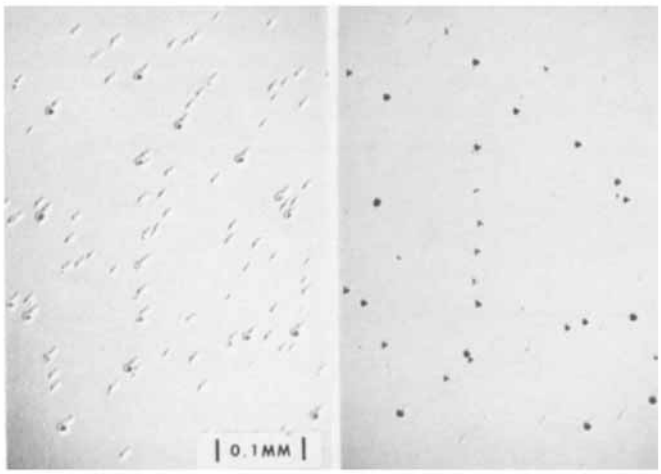


Fig. 9. Parts of unattacked silicon surface remaining after HI/H_2 998°C etch (interference contrast).



a b

Fig. 10. Views of Sirtl-etched layer deposited at 998°C after 998°C HI etching, showing coincidence of faults and outcroppings remaining after etch. (a) Interference contrast, (b) bright field.

layers deposited at 998°C. They were also free from outcroppings, such as those that appear in Figures 8 and 9 and are the forerunners of the faults.

Deposition Test of H_2 and HI/H_2

Slices that had been cleaned by etching at 1,200°C with HCl were exposed to air at room temperature, then etched by either H_2 or HI/H_2 at 998°C and deposited on at 998°C. The H_2-etched slices showed many stacking faults arranged in a manner suggesting incomplete removal of an oxide film (Figure 11). The HI/H_2-etched slices showed no stacking faults or tripyramids. Thus, the HI does remove the oxide layer, and neither it nor the H_2 and the reactor system contribute a sufficient amount of impurities to cause defect difficulties. The deposition process itself is satisfactory at 998°C in our system; therefore, after treatment at 1,200°C with HCl, slices were available that were clean with respect to subsequent etching at 998°C with HI and deposition at the same temperature. These slices could be used to test the various steps in the cleaning procedure.

Deposition Test of Steps in the Cleaning Procedure

Slices cleaned by 1,200°C HCl etching were put through various steps in the cleaning procedure. The sulfuric acid, the 30% hydrogen peroxide, the 50% HF, the water, and the H_2SO_4-H_2O_2 mixture were each tested separately. Slices were either fully immersed in these reagents or partially immersed for a known length of time; then the slices were vapor etched with HI at 998°C, and a 4 μm layer was deposited. In the case of Freon-12, the slices were simply subjected to a gas stream from a dispenser can. Stacking fault and tripyramid distributions and counts on the deposited layers were recorded.

Table 1. Slice Clean-up Steps Tested and Results Obtained by Etching and Deposition at 998°C

Clean-up step tested		Results of deposition
Half immersion in H_2O	PTFE vessel	No stacking faults
	polypropylene	Stacking faults at liquid boundary and lower edge
Half immersed in dilute HF	Run 1	No stacking faults
	Run 2	Some faults at liquid boundary
30% H_2O_2; 15 min DI water		Many stacking faults
Conc. H_2SO_4; 15 min DI water		Intermediate between H_2O_2 and no stacking faults. Perhaps due to polypropylene.
10 parts H_2SO_4 4 parts 30% H_2O_2;	15 min DI water	Better than H_2SO_4 alone
Freon-12 vapor blast		No stacking faults

Fig. 11. Slice cleaned at 1,200°C with HCl, exposed to air, and 998°C H_2-etched before deposition of 3 μm layer.

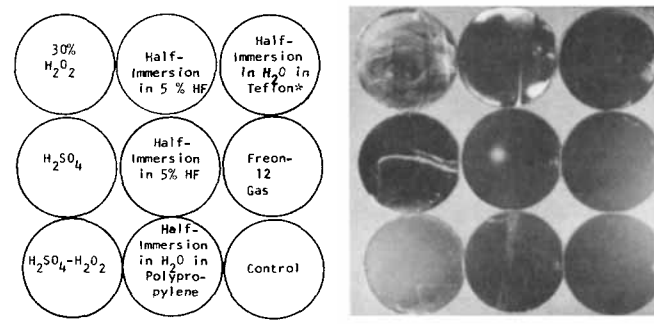


Fig. 12. Slices subjected to various treatments between 1,200°C HCl etching and 998°C HI etching and deposition.

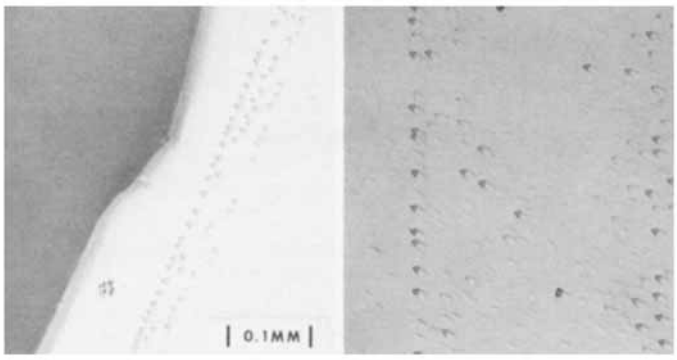


Fig. 13. Stacking faults at edge and center of slice half immersed in water in a polypropylene vessel between etching and deposition.

Table 1 summarizes the cleaning steps tested and the results. Figure 12 shows the appearance of the slices after the deposition test. The main results noted were that the polypropylene vessel used for water and HF rinsing gave off a contaminant film, and that the peroxide was also heavily loaded with a contaminant that presented problems for the 998°C etching and deposition. Figure 13 shows two regions, an edge and the center, of the slice partially immersed in water in a polypropylene vessel before deposition. Stacking faults were arranged in rows in each of these regions, typical of contamination having been left from a film on the water. Replacing the polypropylene vessel with Teflon* eliminated this film.

ACKNOWLEDGMENT

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* Dupont registered trademark.

Controller Design for Distributed Systems via Bass' Technique

THOMAS E. BAKER and COLEMAN B. BROSILOW

School of Engineering
Case Western Reserve University, Cleveland, Ohio 44106

Bass' feedback controller design technique is extended to distributed parameter systems and its use is illustrated for a parabolic system with boundary control.

The development of the design technique rests on a conjecture concerning the necessary and sufficient conditions for the asymptotic stability of linear time invariant partial differential equations. It is shown through a study of the discretized analog of a distributed system that the most likely candidate for a Lyapunov functional general enough to yield the necessary and sufficient conditions for asymptotic stability is a double integral with a symmetric kernel.

The essence of Bass' design technique (*1*) is that it aims to maximize stability and optimize system performance. The control variables are chosen to make the rate of change of a quadratic Lyapunov function as negative as possible, while the parameters of the Lyapunov function are chosen so that the control nearly minimizes a specified quadratic performance index. For linear lumped parameter processes with hard constraints on the control, the design technique proceeds as follows:

Let process equations be given by

$$\frac{dy}{dt} = Ay + Bm \tag{1}$$

where y = an n dimensional vector
m = an m dimensional vector whose elements satisfy $|m_i| \leq k_i$
A = an $n \times n$ real matrix all of whose eigenvalues have negative real parts
B = an $n \times m$ real matrix

The performance criterion to be minimized is $\phi(m)$, where

$$\phi(m) = \int_0^\infty y'Qydt \tag{2}$$

Correspondence concerning this paper should be addressed to C. B. Brosilow. T. E. Baker is with the Department of Control Engineering, Victoria University of Manchester, Manchester, England.